Please amend Claim 1 as follows.

1. (**Currently Amended**) During the testing of the operation of processing unit, a system for identifying the occurrence of an interrupt service routine code flush condition in ~~the~~ a pipeline flattener, the system comprising:

timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream;

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream; and

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus, the periodic signals resulting in periodic sync markers in the timing trace stream and in the program counter trace stream.

wherein the program counter trace apparatus is responsive to an interrupt service routine code flush signal, the program counter trace apparatus generating a sync marker signal group identifying the occurrence of the interrupt service routine code flush signal and relating the interrupt service routine code flush signal to the timing trace stream and to ~~the~~ program code execution.

2. (**As Filed**) The system as recited in claim 1 wherein the marker signal group includes a program counter address, a timing index and a periodic sync ID.

Please amend Claim 3 as follows.

3. (**Currently Amended**) The system as recited in claim 1 further comprising:

a data trace apparatus responsive to signals from the processing unit, the data trace apparatus generating a data trace stream, wherein the periodic signals are applied to the data trace apparatus resulting in periodic sync markers in the data trace stream; and

a host processing unit, the host processing unit responsive to the timing trace stream, the program counter trace stream and the data trace stream, the host processing unit reconstructing the ~~processing activity~~ the program code execution of the processing unit from the trace streams.

Please amend Claim 4 as follows.

4. (**Currently Amended**) The method for communicating an occurrence of an interrupt service routine code flush signal from a target processor unit to a host processing unit, the method comprising:

generating a timing trace stream, a program counter trace stream, and a data trace stream, and

in the program counter trace stream, including an interrupt service routine code flush sync marker signal group indicating an occurrence of an interrupt service routine code flush signal and relating the occurrence to the data trace stream and to the timing trace stream.

5. (**As Filed**) The method as recited in claim 4 further including:

including periodic sync markers in the timing trace stream and in the program counter trace stream; and

including in the program code sync marker reference to a periodic sync marker.

Please amend Claim 6 as follows.

6. (**Currently Amended**) In a processing unit test environment wherein a target processor transmits a plurality of trace streams to a host processing unit, an interrupt service routine code flush sync marker signal group included in a trace signal stream, the target processor including a target processor clock, the marker signal group comprising:

an indicia of the occurrence of an interrupt service routine code flush signal;

an indicia of the relationship of the occurrence of the interrupt service routine code flush signal to the target processor clock; and

an indicia of the relationship of the occurrence of the interrupt service routine code flush signal to ~~the~~ a target processor program execution.

Please amend Claim 7 as follows.

7. (**Currently Amended**) In a target processing unit generating trace test signals for transfer to a host

processing unit, a program counter trace generation apparatus comprising:

sync marker assembly apparatus, the sync marker assembly apparatus including:

a storage unit;

a decoder unit responsive to an interrupt service routine code flush signal for storing an indicia of ~~the~~ an interrupt service routine code flush signal in the storage unit, the decoder unit generating a ~~controls~~ control signal;

a gate unit having a timing index, a periodic sync signal, and a program counter address, the gate unit storing the timing index, the periodic sync signal and the program counter address in the storage unit; and

a FIFO unit, the storage unit transferring the stored signals to the FIFO unit in the form of a program code flush sync marker.

8. **(As Filed)** The program counter trace apparatus as recited in claim 7 responsive to a selected control signal for transferring the interrupt service routine code flush marker in the FIFO unit to an output port of the target processor.

9. **(As Filed)** The program counter trace apparatus as recited in claim 8 wherein the apparatus can form a periodic sync marker in response to a periodic sync signal.

Please amend Claim 10 as follows.

10. (**Currently Amended**) The program counter trace apparatus as recited in claim 9, wherein the target procession unit includes a pipeline flattener, wherein the interrupt service routine flush signal indicates the change from a first instruction code sequence to a second instruction code sequence exiting the pipeline flattener.

11. (**As Filed**) The program counter trace apparatus as recited in claim 10 wherein the first instruction code sequence is an interrupt service routine code and the second instruction sequence is a program code.